

WE CLAIM:

- 5 1. A overcurrent protection circuit for a motor drive circuit, comprising:
a first FET having a gate input and conducting a motor current of the motor, a
drain and a source;
a second FET having a gate input coupled to said first FET input gate and
conducting a bias current, a drain and a source; and
a comparator coupled across said drains of said first FET and said second FET
and providing an output indicative of a voltage across said comparator inputs.
- 10 2. The overcurrent protection circuit of Claim 1 wherein each said first FET gate and
said second FET gate are driven hard by a voltage to generate a low on resistance between
the respective source and drain.
- 15 3. The overcurrent protection circuit of Claim 2 wherein said bias current is variable
to responsively adjust a threshold voltage of said comparator.
- 20 4. The overcurrent protection circuit of Claim 3 wherein said second FET drain is
coupled to a non-inverting input of said comparator.
5. The overcurrent protection circuit of Claim 4 wherein said first FET drain is
coupled to an inverting input of said comparator.
6. The overcurrent protection circuit of Claim 2 wherein said FET drive voltage is
25 generated by a voltage pump.
7. The overcurrent protection circuit of Claim 6 wherein said voltage pump is a
voltage doubler.

8. The overcurrent protection circuit of Claim 1 wherein a ratio of said motor current to said bias current is proportional to a size of said first FET with respect to a size of said second FET.

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9. The overcurrent protection circuit of Claim 1 wherein said bias current is selectively programmable.

10. The overcurrent protection circuit of Claim 9 wherein said bias current is digitally programmable.

11. The overcurrent protection circuit of Claim 1 wherein said comparator generates said output being indicative of said motor current exceeding said a predetermined threshold and being a function of said bias current.

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12. The overcurrent protection circuit of Claim 1 wherein said comparator has delay circuitry filtering out any transient current spikes through said first FET.

13. The overcurrent protection circuit of Claim 1 wherein said first FET is in parallel with said second FET.

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